

Aging in RF Design: Long-Term Reliability and Performance Degradation Over Time

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Abstract – Long-term reliability of radio-frequency integrated circuits remains a practical concern that is sometimes overlooked during initial design phases, especially in cost-sensitive applications where design margins tend to be minimal. This paper reviews the main mechanisms behind performance degradation in RF circuits (Bias Temperature Instability, Hot Carrier Injection, electromigration, and Time-Dependent Dielectric Breakdown) with focus on how these phenomena affect gain, noise figure, and linearity over time. To illustrate these effects, we conducted a simulation study using QUCS-S with a simple common-source amplifier, varying the threshold voltage to mimic aging-induced parameter shifts. Within the scope of this work, this approach provides insight into expected performance trends, though it does not capture all aspects of real aging. We also discuss practical mitigation strategies that can help extend circuit lifetime.

Index Terms—RF circuits, aging, reliability, CMOS, BTI, HCI, electromigration, TDD, simulation

I. INTRODUCTION

When designing RF circuits, engineers typically focus on meeting performance specifications at the time of production. However, how these circuits will behave after years of operation is equally important, though perhaps less often addressed in detail during initial design. Aging-related degradation is particularly problematic because it happens gradually (a circuit may slowly drift out of specification without obvious warning signs).

The situation becomes more complicated as transistor dimensions shrink. Smaller devices mean thinner oxides and higher electric fields, which tend to accelerate some degradation mechanisms even when supply voltages are reduced. Quantifying the exact impact on a specific RF design remains challenging in practice.

In this paper, we examine aging from both theoretical and practical angles. After reviewing the main degradation mechanisms in Section II and their impact on RF performance in Section III, we describe a simulation approach using QUCS-S in Section IV. Section V covers mitigation strategies, and Section VI offers concluding remarks. Within the scope of this work, our goal is not to provide definitive lifetime predictions, but rather to demonstrate a methodology that can help designers consider aging during the design phase.

II. AGING MECHANISMS IN RF TRANSISTORS

Reliability of RF circuits is fundamentally determined by transistor stability. In CMOS technology, several distinct physical mechanisms contribute to device degradation over time. Understanding these mechanisms is essential for predicting circuit behavior and designing circuits with long-term reliability.

A. Bias Temperature Instability (BTI)

Bias Temperature Instability is probably the most discussed aging mechanism in recent literature, though its practical impact is not always easy to quantify. BTI manifests as a shift in threshold voltage (V_{th}) of transistors subjected to voltage stress at elevated temperatures. Although the underlying physics involves complex interactions at the oxide interface, in most circuit simulations (including ours) the effect is reduced to a simple V_{th} shift (a simplification that works reasonably well for first-order analysis). The phenomenon exists in two variants: Negative BTI (NBTI) affecting PMOS devices, and Positive BTI (PBTI) affecting NMOS devices.

NBTI occurs when a PMOS transistor operates in its normal “on” state (gate at negative voltage relative to source and drain). This creates defects at the Si-SiO₂ interface that can capture charge carriers, which shifts the threshold voltage in the negative direction (increasing $|V_{th}|$) and reduces the drive current.

The time evolution of threshold voltage shift due to NBTI is commonly described by a power-law relationship:

$$\Delta V_{th}(t) = A \cdot \exp\left(\frac{-E_a}{kT}\right) \cdot t^n \quad (1)$$

where A is a process-dependent constant, E_a is the activation energy (typically 0.1–0.2 eV), k is Boltzmann’s constant, T is absolute temperature, t is stress time, and n is the time exponent (typically 0.1–0.25 for NBTI).

PBTI in NMOS devices causes similar threshold voltage shifts, but the mechanism is different: instead of creating interface defects, electrons become trapped directly in the gate oxide.

One aspect of BTI that makes it tricky to characterize is its partial reversibility. If stress is removed and then the threshold voltage is measured, some of the shift will have already recovered. This means that the measured degradation depends on how quickly the measurement can be performed after removing stress.

B. Hot Carrier Injection (HCI)

Hot Carrier Injection occurs when charge carriers in transistor channel gain sufficient kinetic energy from lateral electric field to overcome potential barrier at Si-SiO₂ interface and become injected into gate oxide. These carriers can become trapped in oxide and each injection leaves behind a small amount of permanent damage. Over the device lifetime, this damage accumulates, which is why HCI is classified as an aging mechanism.

This phenomenon is most severe near drain end of channel, where electric field reaches its maximum. For this reason, HCI damage typically manifests as asymmetric degradation.

HCI degradation depends on the gate-to-drain voltage and is often assessed through the substrate current, which indicates the presence of hot carriers. The most critical HCI stress usually happens when the gate voltage is close to the threshold voltage, because this condition produces the highest substrate current.

The impact of HCI on RF circuits extends beyond simple threshold voltage shifts. The localized nature of the damage near the drain creates additional parasitic capacitances and resistances that affect high-frequency performance. Furthermore, the asymmetric degradation can cause differential circuits to become unbalanced over time.

C. Electromigration

Electromigration is the transport of material caused by the gradual movement of ions in a conductor due to momentum transfer between conducting electrons and diffusing metal atoms. Over time, atoms migrate from some locations (leaving voids) to other locations (forming hillocks), leading to eventual interconnect failure.

In RF circuits, electromigration presents particular challenges in power amplifier output stages, where high current densities are common. Additionally, the AC nature of RF signals introduces complexity (while average current determines the steady-state atom migration, peak currents can exceed DC electromigration limits by factors of two or more without causing immediate failure, due to the reversing nature of the current).

D. Time-Dependent Dielectric Breakdown (TDDB)

Time-Dependent Dielectric Breakdown refers to the gradual degradation and eventual failure of gate oxide under continuous electric field stress. Unlike the other mechanisms discussed, TDDB represents an eventual hard failure rather than gradual parametric drift (once breakdown occurs, the transistor typically becomes nonfunctional).

While HCI involves carriers entering the oxide from outside and causing gradual damage, TDDB is fundamentally different (it is the oxide itself slowly developing internal defects until a conductive path forms and the device fails catastrophically).

One practical concern with modern technology is that gate oxides have become progressively thinner. This is problematic for TDDB because, for a given voltage, thinner oxide means stronger electric field (and stronger field accelerates

breakdown). The introduction of high- κ dielectric materials has helped somewhat, since they allow the physical oxide to be thicker while still providing the same electrical capacitance.

III. IMPACT ON RF PERFORMANCE

Device degradation causes measurable changes in RF circuit performance. The exact effects depend on the circuit type and application, but some common trends can be observed.

A. Gain Degradation

Transistor gain in RF applications depends critically on transconductance (g_m), which relates changes in drain current to changes in gate voltage:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \quad (2)$$

Both BTI-induced threshold voltage shifts and HCI-induced mobility degradation directly reduce transconductance. For a threshold voltage increase of ΔV_{th} , the transconductance at a fixed gate voltage decreases by:

$$\Delta g_m = -\mu C_{ox} \frac{W}{L} \Delta V_{th} \quad (3)$$

In a typical common-source amplifier, the voltage gain at low frequencies is approximately $A_v \approx g_m \cdot R_L$, where R_L represents the load impedance. Thus, threshold voltage degradation translates directly into gain loss.

At higher frequencies (typically above 1 GHz), parasitic elements become significant and the simple $g_m \cdot R_L$ approximation breaks down, requiring full S-parameter analysis. Still, transconductance degradation remains the dominant factor affecting amplifier gain over time.

B. Noise Figure Degradation

The noise figure of RF amplifiers depends on multiple device parameters, including transconductance, gate resistance, and the thermal noise generated in the channel. In general, anything that degrades the transistor's ability to amplify the signal while adding its own noise contribution will have a negative impact on the noise figure.

Aging affects noise figure through various factors. Reduced transconductance means the transistor provides less gain, so noise from subsequent stages becomes more significant when referred to the input. Additionally, interface traps created by BTI and HCI contribute additional noise sources which are not present in fresh devices. The generation-recombination noise from these traps can be particularly significant at lower frequencies, contributing to increased flicker noise corner frequency.

C. Linearity Degradation

Aging degrades amplifier linearity. The damage caused by HCI is not uniform across the transistor channel, which introduces additional distortion. For RF amplifiers that must handle both weak and strong signals, this can be problematic (metrics like the 1-dB compression point (P1dB) typically degrade with aging).

D. Frequency Response Changes

Every transistor has a maximum frequency at which it can effectively amplify signals. This limit is called the unity-gain frequency (f_T):

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (4)$$

Aging affects both g_m and capacitances: g_m decreases due to threshold voltage shift, and trapped charges add extra capacitance. Both effects reduce f_T . For circuits like oscillators that must operate at a specific frequency, changes in transistor capacitances shift the oscillation frequency, potentially moving the circuit outside its intended frequency band.

IV. SIMULATION METHODOLOGY

To illustrate the effects of aging on RF performance, we simulated a simple amplifier circuit and varied the threshold voltage to represent different stages of device degradation.

A. Simulation Platform

For this work we used QUCS-S (Quite Universal Circuit Simulator with SPICE support) with Ngspice as the simulation backend. QUCS-S provides a graphical interface for circuit design and supports S-parameter simulation, which is needed for RF circuits.

Since QUCS-S does not have built-in aging models, we simulated the effect of aging by manually varying the threshold voltage parameter.

B. Test Circuit: Common-Source RF Amplifier

For this study, we chose a basic common-source MOSFET amplifier. A simple circuit topology was chosen to make the aging effects easier to observe (real low-noise amplifiers would typically include input/output matching networks and possibly inductive source degeneration for noise optimization). However, the common-source topology captures the essential relationship between transistor parameters and amplifier gain, which is what we wanted to demonstrate within the scope of this work.

Fig. 1 shows our test circuit. It consists of an NMOS transistor (M1) with resistive biasing:

- Gate bias set by R1/R2 voltage divider
- Source resistor R_s with bypass capacitor C_s
- Drain load resistor R_d
- Coupling capacitors C_{in} and C_{out} for DC blocking
- RF choke L_d in the drain supply path

The nominal design parameters are listed in Table I.

C. MOSFET Model and Aging Representation

As already mentioned, we varied the threshold voltage parameter (V_{th}) in Ngspice's MOSFET model to represent the combined effect of BTI and HCI. The transistor model used was a standard Level 1 MOSFET with channel width $W = 120 \mu\text{m}$ and length $L = 0.4 \mu\text{m}$.

This is a simplified approximation. Real aging also affects mobility, oxide capacitance, and introduces additional parasitic elements that we are not capturing. The threshold voltage

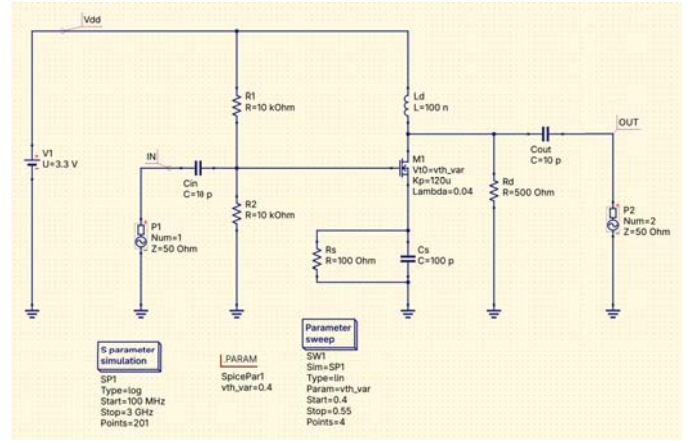


Fig. 1. Common-source RF amplifier schematic in QUCS-S with S-parameter simulation and parameter sweep configuration for aging study.

TABLE I. Component Values for Test Amplifier

Component	Symbol	Value
Input coupling capacitor	Cin	10 pF
Output coupling capacitor	Cout	10 pF
Gate bias resistor (upper)	R1	10 kΩ
Gate bias resistor (lower)	R2	10 kΩ
Drain load resistor	Rd	500 Ω
Source degeneration resistor	Rs	100 Ω
Source bypass capacitor	Cs	100 pF
Drain inductor	Ld	100 nH
Supply voltage	Vdd	3.3 V

shift is the most commonly discussed effect and the easiest to implement in a parametric sweep, which is why we focused on it for this study.

We used V_{th} values ranging from 0.40 V (representing a fresh device) to 0.55 V (representing significant aging). Whether these numbers correspond to 5 years or 15 years of operation depends heavily on the specific technology and operating conditions (without access to foundry reliability data, these values are approximate and serve to illustrate trends rather than provide absolute lifetime predictions).

D. Simulation Results and Observations

Fig. 2 shows the S21 (gain) curves from our simulation over a frequency range of 100 MHz to 3 GHz. As expected, the gain decreases when threshold voltage increases.

The absolute gain values in our simulation are low (on the order of -40 dB) because the circuit has no impedance matching. However, what matters here is not the absolute value but the relative change with aging.

Based on our simulations, even a small change in threshold voltage (50 mV) causes visible gain reduction. At 2 GHz, for example, the gain magnitude decreases from approximately -40.7 dB for the fresh device ($V_{th} = 0.40$ V) to approximately -41.6 dB for the most aged condition ($V_{th} = 0.55$ V), representing a relative reduction on the order of 10%. In practice, this means the amplifier should be designed with some reserve gain to compensate for aging, though the exact margin depends on the specific application and expected lifetime.

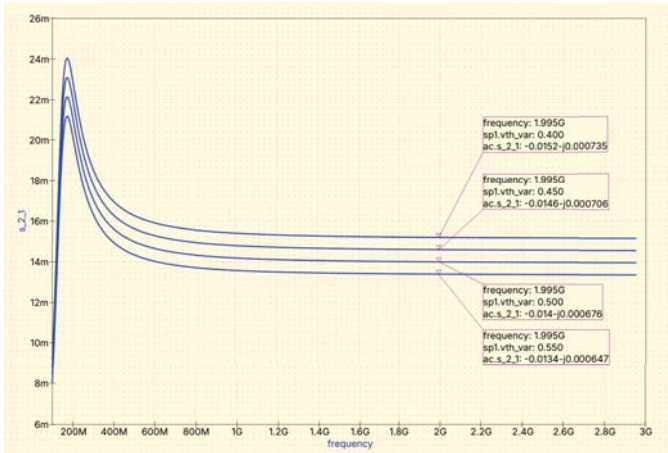


Fig. 2. Simulated S21 versus frequency for threshold voltage values of 0.40 V (fresh device), 0.45 V, 0.50 V, and 0.55 V (aged device). Curves from top to bottom correspond to increasing V_{th} .

V. MITIGATION STRATEGIES

Since aging cannot really be avoided (it is a physical reality of semiconductor operation), the practical question for designers is how to deal with it. Either you slow it down through careful operating point selection, or you design circuits that can tolerate some degradation without failing specifications. Several approaches are commonly used.

A. Adding Performance Margins

The most straightforward approach is to design circuits with enough margin so they still meet specifications after years of aging. If simulations indicate 2 dB gain loss over projected lifetime, initial design should provide 2 dB additional gain above minimum specification.

This approach has limitations. Excessive margin requires larger transistors operating at higher bias currents, which increases power consumption. In battery-powered applications, this tradeoff may be unacceptable.

B. Bias Point Optimization

How fast a transistor ages depends on the operating conditions. Higher voltages and higher temperatures cause faster degradation. For the chosen bias point, careful selection of operating conditions can slow down the aging process.

For RF amplifiers, practical approaches include using lower bias voltages when possible, reducing bias current when the amplifier is not handling strong signals, and good thermal design to prevent overheating. The tradeoff is typically between performance and lifetime.

C. Redundancy and Reconfiguration

In critical systems, one approach is to have backup signal paths that can be used when the main path degrades too much. More advanced systems continuously monitor their own performance and automatically adjust settings to compensate for aging.

A simpler version of this is adaptive biasing, where a feedback circuit adjusts the bias voltages to keep the amplifier performance constant even as the transistors degrade.

D. Technology Selection

Not all transistor technologies age the same way. For example, Silicon-on-Insulator (SOI) transistors are generally more resistant to hot carrier damage. Wide-bandgap semiconductors like GaN and SiC can handle higher temperatures and voltages, which makes them popular for power amplifiers. For applications that need to work reliably for many years, it is worth considering which technology is most resistant to the expected degradation mechanisms.

VI. ASSUMPTIONS AND LIMITATIONS

It is important to be clear about what this simulation can and cannot tell us.

The most obvious limitation is that we only varied one parameter. In a real aging scenario, threshold voltage shift would be accompanied by mobility degradation, changes in oxide capacitance, increased gate leakage, and probably some amount of interconnect degradation as well. Capturing all of this would require much more sophisticated modeling, which was beyond the scope of this work.

Another issue is that we have no way to correlate our V_{th} values to actual operating time without access to reliability data from a specific foundry process. The numbers we used (0.40 V to 0.55 V) are approximate (they might represent 5 years in one technology or 20 years in another, depending on operating conditions, temperature, etc.).

We also simplified by assuming constant stress conditions. In reality, RF signals constantly change amplitude, so the stress on transistors varies over time. Also, some degradation mechanisms (like BTI) partially recover when the device is not under stress. This means that devices which are turned off periodically may age more slowly than devices running continuously.

For this demonstration, including a simple input matching network could have provided more realistic absolute gain values, but this was intentionally omitted to keep the focus on relative degradation trends. Despite these simplifications, this approach demonstrates that small changes in transistor parameters affect amplifier performance. This work demonstrates how reliability can be integrated into the design process from the beginning, rather than being evaluated only as a final check.

VII. CONCLUSION

We have reviewed the main aging mechanisms relevant to RF CMOS circuits and illustrated their effects through a simulation exercise. The four mechanisms discussed (BTI, HCI, electromigration, and TDDDB) each contribute to gradual performance degradation.

Two natural extensions of this work would be: (1) incorporating factory reliability data to directly map threshold voltage shifts to operating lifetime, and (2) analyzing a more realistic

amplifier topology with proper input and output matching networks to comprehensively assess how aging affects gain, input matching, noise figure, and overall circuit performance.

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